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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,845	01/23/2001	Kiyotoshi Ueda	50090-265	1553

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EXAMINER
PATEL, PARESH H

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/766,845	Applicant(s) UEDA ET AL.	
	Examiner Paresh Patel	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *6 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7-9,11,13 and 14* is/are rejected.

7)☒ Claim(s) *4,10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election of Species 1 of fig. 4 (Claims 1-11 and 13-14) in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim 6, which recites the limitation of non-elected Species 2 has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Tamaki (US 6061282).

Regarding claim 7, Tamaki discloses: A semiconductor integrated circuit testing apparatus [fig.1] comprising correcting means [2, 3, 5 of fig. 1] for correcting input waveform timing of a measure signal [lines 65-67 of col. 4, lines 1-3 of column 5, lines

33-41 of column 5 and fig. 5] applied to all pins [lines 23-26 of column 4] of a semiconductor integrated circuit [3 of fig. 2].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 8, 9, 11, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki as applied to claim 7 above, and further in view of Ungar (US 5563524).

Regarding claim 8, Tamaki discloses: said correcting means includes:

latching means [32] for latching said measuring signal by use of said clock signal from said clock generating means;

storing means [31] for storing as data said measuring signal latched by said latching means. and

controlling means [lines 7-10 of column 4] for retrieving the data held in said storing means for output to an external entity.

Tamaki discloses all the essential elements of the claimed invention except for a clock generating means for generating a clock signal. Rather, Tamaki discloses clock buffer [5] which receives clock signal from an external clock. However, Ungar discloses a clock generating means [12 and TCK of fig. 2] for generating a clock signal. It would

have been obvious to one having ordinary skill in the art at the time the invention was made to modify the testing apparatus of Tamaki with clock generating means of Ungar in order to make universal test apparatus [lines 61-67 of column 1] for testing electrical circuits [lines 32-37 of column 1 and fig. 1].

Regarding claim 9, Tamaki discloses: said latching means [32], said storing means [31] and said controlling means [lines 7-10 of column 4] are incorporated in said semiconductor integrated circuit [1 of fig. 1].

Regarding claim 11, Ungar discloses: said clock generating means is a high-speed clock generating circuit for generating a high-speed clock signal [12].

Regarding claim 14, Tamaki discloses: the semiconductor integrated circuit fabricated by use of a semiconductor integrated circuit testing apparatus [fig. 1].

Regarding claims 1-3, 5 and 13, clearly the above testing apparatus of Tamaki and Ungar in combination will provide recited method steps.

Allowable Subject Matter

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art does not teach or suggest a semiconductor integrated circuit testing apparatus comprising correcting means for correcting input waveform timing of a measure signal applied to all pins of a semiconductor integrated circuit; wherein said

correcting means include latching means for latching said measuring signal by use of said clock signal from said clock generating means; storing means for storing as data said measuring signal latched by said latching means; and a controlling means for retrieving the data held in said storing means for output to an external entity; wherein said latching means is constituted by terminating circuits and latch circuits, and said storing means by FIFO memories and scan FF circuits.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art does not teach or suggest a semiconductor integrated circuit testing method comprising the steps of: causing a tester to generate a measuring signal to all pins of a semiconductor integrated circuit; generating a trigger signal; latching said measuring signal by use of said trigger signal; storing the latched measuring signal as data into storing means; reading the stored data from said storing means for output to said tester; creating a calibration data file based on the data sent to said tester; referencing said calibration data file to correct waveform timing of said measuring signal upon functional test performed by said tester.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
July 13, 2002

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800